REMARKS

Thorough examination and careful review of the application by the Examiner is noted and appreciated.

Claims 28-30 are pending in the application. Claims 28-30 stand rejected.

Claim 29 has been amended to correct a typographical error. Such correction is supported by the disclosure in claims 28 and 30.

Claim Rejections Under 35 USC §103

Claims 28-30 are rejected under 35 USC §103(a) as being unpatentable over Uzoh et al '376 in view of Chidambarrao et al '572. It is contended that Uzoh discloses the claimed damascene interconnect formed by a trench-filling process of electroplating copper including the range of copper grain size as claimed. It is further contended that while Uzoh does not teach a decrease in electrical resistance, such is taught by Chidambarrao in disclosing a relationship between the electrical resistance and the grain size as it relates to the voids in the interconnect.

The rejection of claims 28-30 under 35 USC §103(a) based on Uzoh et al and Chidambarrao et al is respectfully traversed.

Uzoh et al discloses a method and structure for improving electromigration of chip interconnects wherein a microstructure including a conductive layer of aluminum, copper or alloys thereof on a substrate wherein the layer including metal grains at least about 0.1 microns and barrier material. (See Abstract)

At col. 4, lines 4-11, Uzoh et al further states:

> "Large grains are always preferably to small grains, as grain boundaries present a fast-diffusion path for electromigration or stress migration (both are interconnect wear out mechanisms). Therefore larger grained damascene interconnects have higher reliability when all other factors are equal. **A typical average aluminum grain size (for fill in submicron trenches) is on order of 0.5 micron, in a lognormal distribution.**"

The present invention, on the other hand, recites a semiconductor structure having interconnects formed of copper with grain size **not less than 0.5 μm** and **a decrease in electrical resistance of at least 15% after a time period of not more than 30**

hours at about 21°C, as clearly recited in independent claim 28. Contrary to the teaching of Uzoh et al that the average grain size is 0.5 micron, the present invention teaches and claims a grain size of not less than 0.5 micron. Furthermore, no where in Uzoh is taught the unexpected result only discovered by the present invention of having a decrease in electrical resistance of at least 15%.

Chidambarrao et al discloses a process for producing metal interconnections and product in which a process for producing a multi-level semiconductor device that has metal interconnections with insulating passivation layers is disclosed. At col. 4, lines 8-33, Chidambarrao et al states:

> "Methods of reducing the effect of void formation on the electrical resistance of interconnect conductors in multi-level metallization structures having provided by incorporating multiple continuous redundant conductive layers ... Typically, the grain size of the redundant underlayer or overlayer of a multi-layer conductor is much less than the width of the conducting interconnect..."

The Applicants respectfully submit while Chidambarrao et al discussed the general principal of reducing the effect of void formation on the electrical resistance of interconnect conductors, Chidambarrao et al does not specifically teach, as now recited in independent claim 18:

> "interconnect formed by a trench-filling process of electroplated Cu having an as-deposited **grain size of not less than 0.5 μm** and a **decrease in electrical resistance of at least 15% after a time period of not more than 30 hours at about 21°C.**"

The Applicants respectfully submit that, contrary to the Examiner's contention that Chidambarrao et al shows the relationship between the electrical resistance and the grain size, such relationship is not shown by Chidambarrao and is only shown by the present invention as recited in independent claim 28.

In the Response to Arguments Section of the 11/04/2004 Office Action, the Examiner further argued that "the reference while teaching the average grain size of 0.5 microns further teaches as recited in the remarks, that 'large grains are always preferable to small grains'. Thus one having ordinary skill in the

art would have been motivated to maintain the grain size at 0.5 micron or larger".

The Applicants respectfully submit that such reasoning does not support a §103(a) obviousness rejection since Uzoh teaches that **the average grain size of 0.5 microns, and Uzoh does not teach the minimum grain size of 0.5 microns**, which is only taught by the present invention. When the average grain size is 0.5 microns, then the minimum grain size must be smaller than 0.5 microns taught by Uzoh. The Applicants therefore respectfully submit that it is only the present invention that teaches a minimum grain size must be 0.5 microns, and that, any grain size at less than 0.5 microns would not work. The Applicants therefore respectfully conclude that the minimum grain size of 0.5 microns is clearly not taught by Uzoh.

The Examiner further argued that "the Chidambarrao patent teaches that by selection of grain size and reducing void formation, electrical resistance may be controlled (see col. 4, lines 8-33)." The Applicants respectfully submit that such teaching does not even come close to the present invention's teaching of "a decrease in electrical resistance of at least 15%

after a time period of not more than 30 hours at about 21°C." In other words, the present invention clearly defined limitation can not be inferred from the vague and indefinite statement of Chidambarrao.

The rejection of claims 28-30 under 35 USC §103(a) based on Uzoh et al and Chidambarrao et al is respectfully traversed. A reconsideration for allowance of these claims is respectfully requested of the Examiner.

Based on the foregoing, the Applicants respectfully submit that all of the pending claims, i.e. claims 28-30, are now in condition for allowance. Such favorable action by the Examiner at an early date is respectfully solicited. In the event that the present invention is not in a condition for allowance for any other reasons, the Examiner is respectfully invited to call the Applicants' representative at his Bloomfield Hills, Michigan office at (248) 540-4040 such that necessary action may be taken to place the application in a condition for allowance.

Respectfully submitted,

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